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In re Application of

Harari

Application Number

07/337,566

Filed

APR. 13, 89

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Harari et al.

[45] **Date of Patent:** Feb. 17, 1998

[54] FLASH EEPROM SYSTEM

63-183700 7/1988 Japan .
63-225999 9/1988 Japan .

[75] Inventors: **Eliyahou Harari**, Los Gatos; **Robert D. Norman**, San Jose; **Sanjay Mehrotra**, Milpitas, all of Calif.

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[73] Assignee: **SanDisk Corporation, Sunnyvale, Calif.**

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[21] Appl. No.: 407,916

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[22] Filed: Mar. 21, 1995

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Related U.S. Application Data

[60] Continuation of Ser. No. 963,851, Oct. 20, 1992, Pat. No. 5,418,752, which is a division of Ser. No. 337,566, Apr. 13, 1989, abandoned.

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[51] Int. CL⁶ G11C 11/34

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[52] U.S. Cl. 365/185.33; 365/185.22;
365/185.29

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[58] **Field of Search** 365/185, 218,
365/900, 230.03, 104, 185.22, 185.29, 185.33

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Primary Examiner—Joseph A. Popek

Attorney, Agent, or Firm—Majestic, Parsons, Siebert & Hsue

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[57] **ABSTRACT**

(List continued on next page.)

A system of Flash EEPROM memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. Yet another improvement is the use of a write cache to reduce the number of writes to the Flash EEPROM memory, thereby minimizing the stress to the device from undergoing too many write/erase cycling.

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23 Claims, 5 Drawing Sheets

